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MS-7821

Intel -Shark Bay plamform Z87

ATX

Ver: 12

CPU:

System Chipset:

Marswell LGA1150

Lynx Point

Onboard Chip:

HD Audio Codec:ALC1150

LAN-Killer E2205

SIO:Fintek NTC6799D

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (800/1066/1333MHz) * 4 (Dual Channel)

ACPI:

PWM:

UPI

VRD12 -UP1649-8Phase

Expansion Slots:

Other:

PCI Express (X16) Slot *3

SATA3.0 x6 (PCH)

PCI Express (X1) Slot * 4

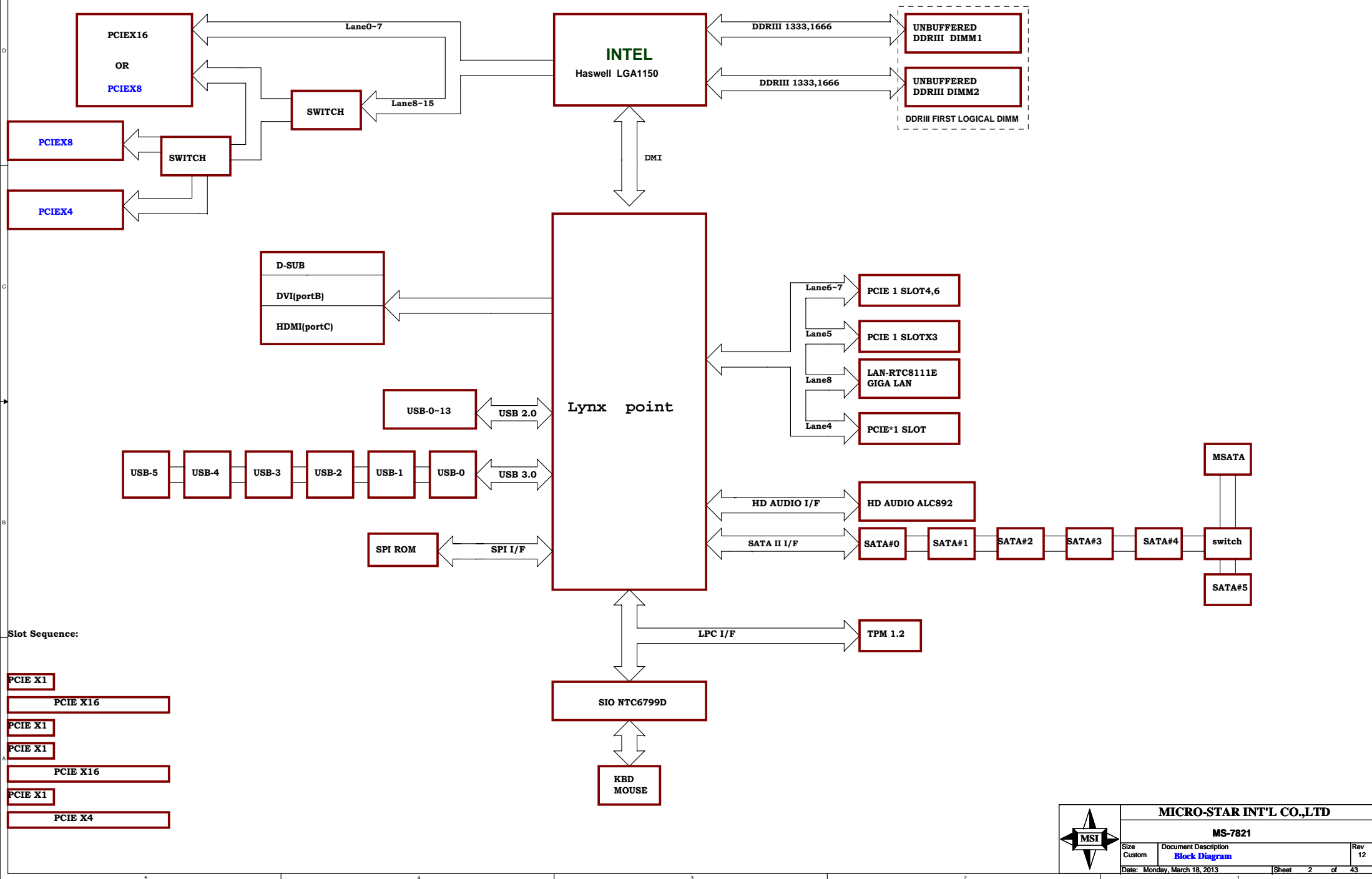
REAR USB2.0 *2

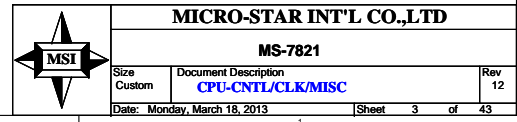
FRONT USB2.0 *6

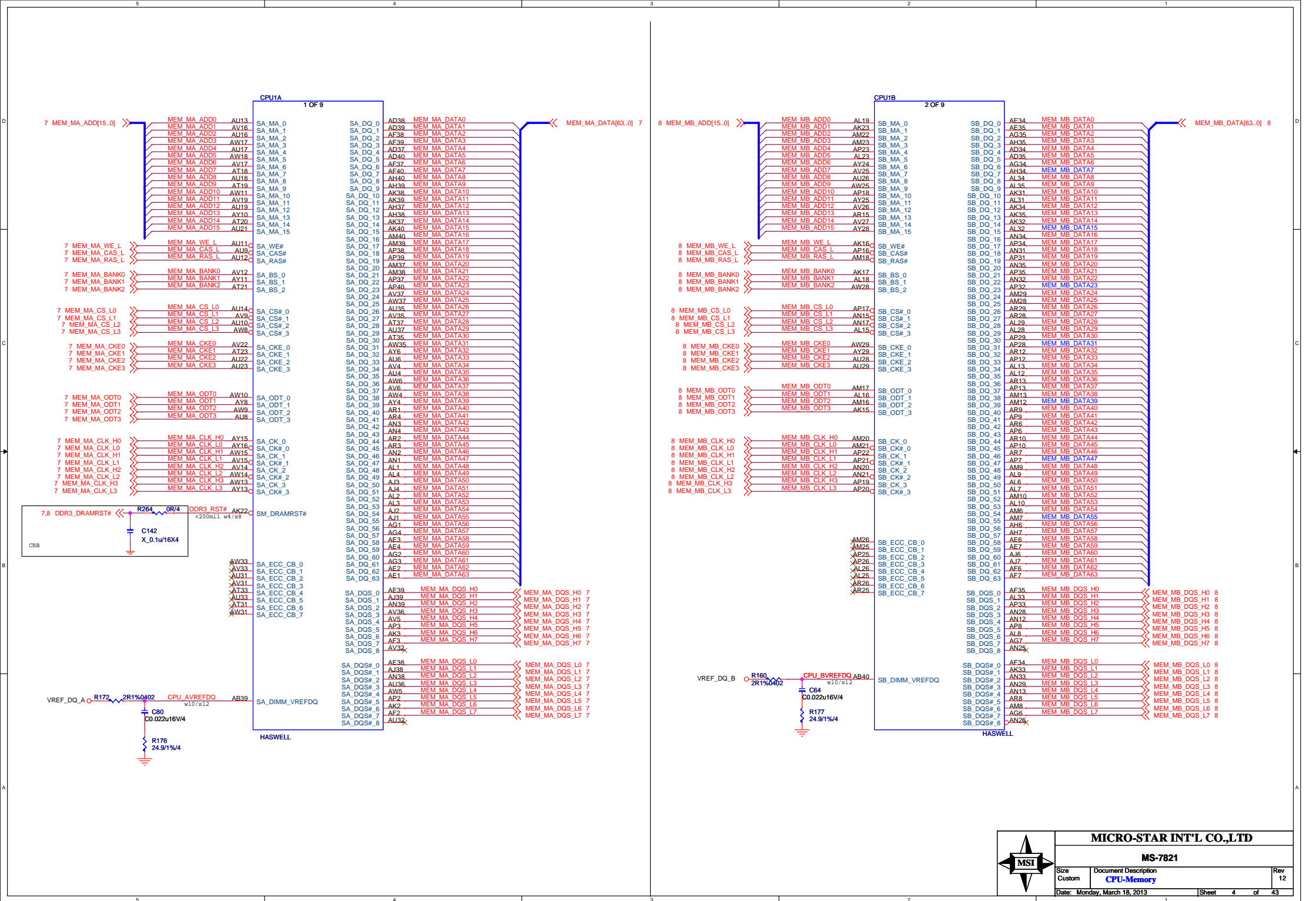
REAL USB3.0 *4

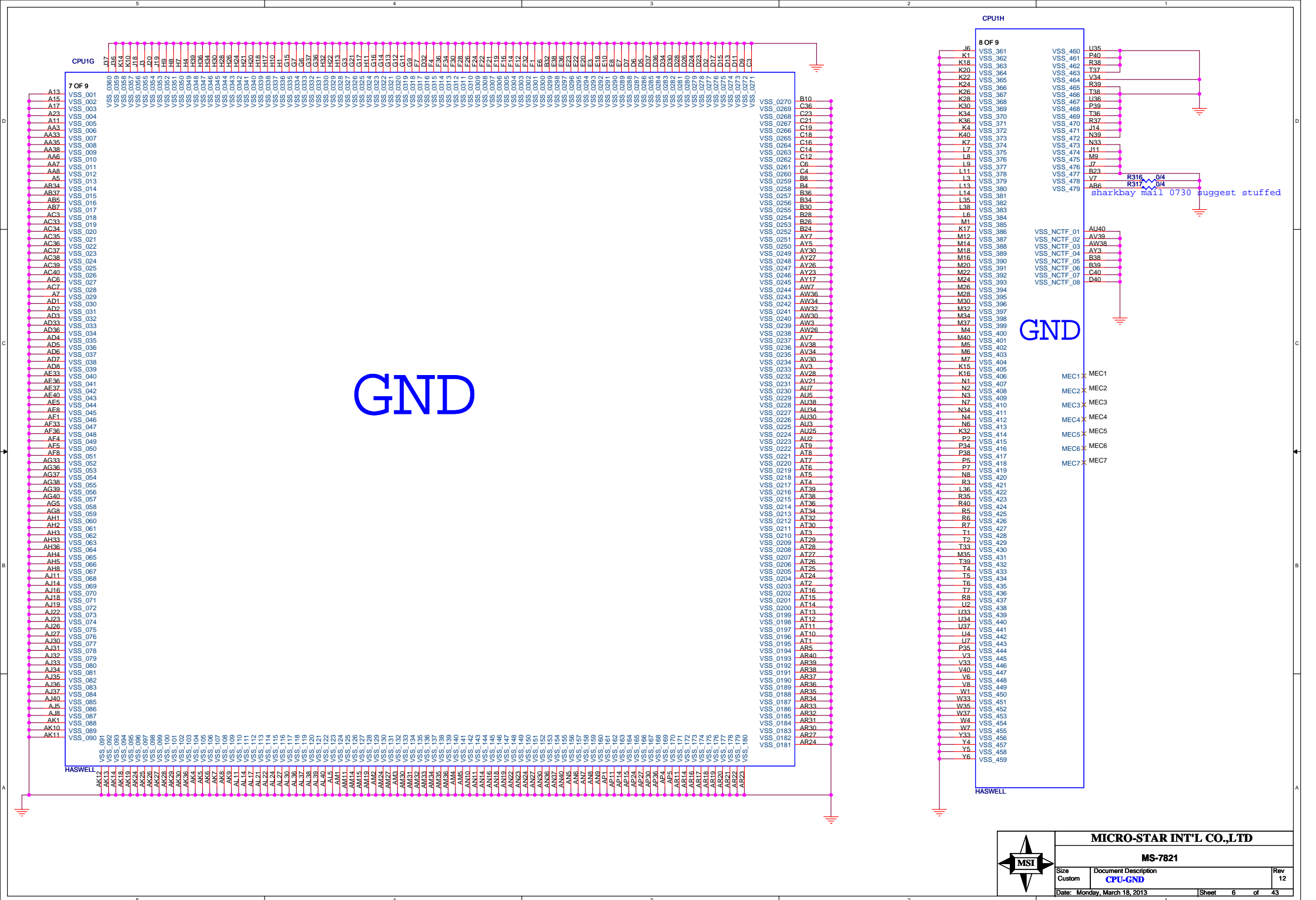
FRONT USB3.0 *2

MS-7821 Block Diagram



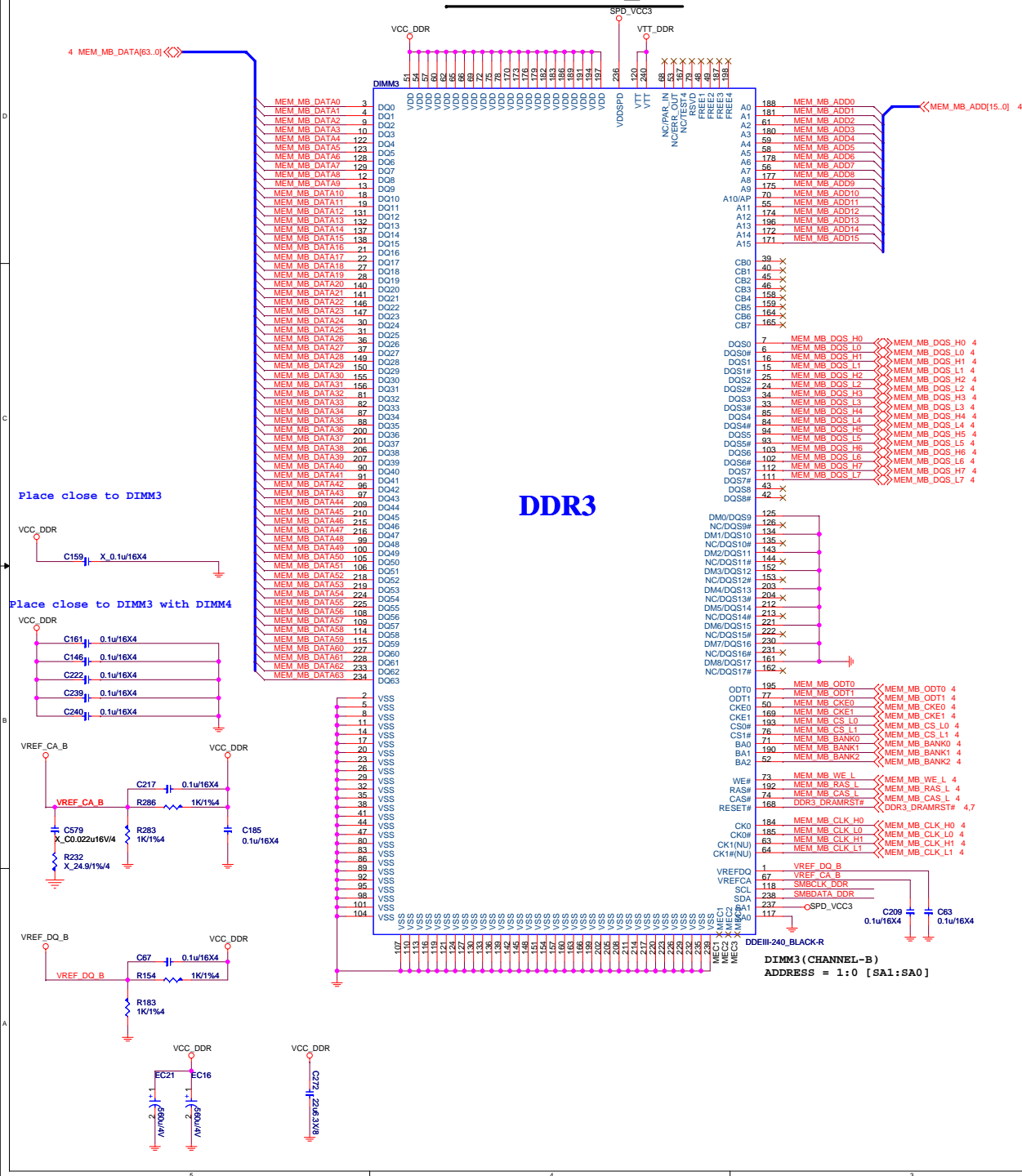




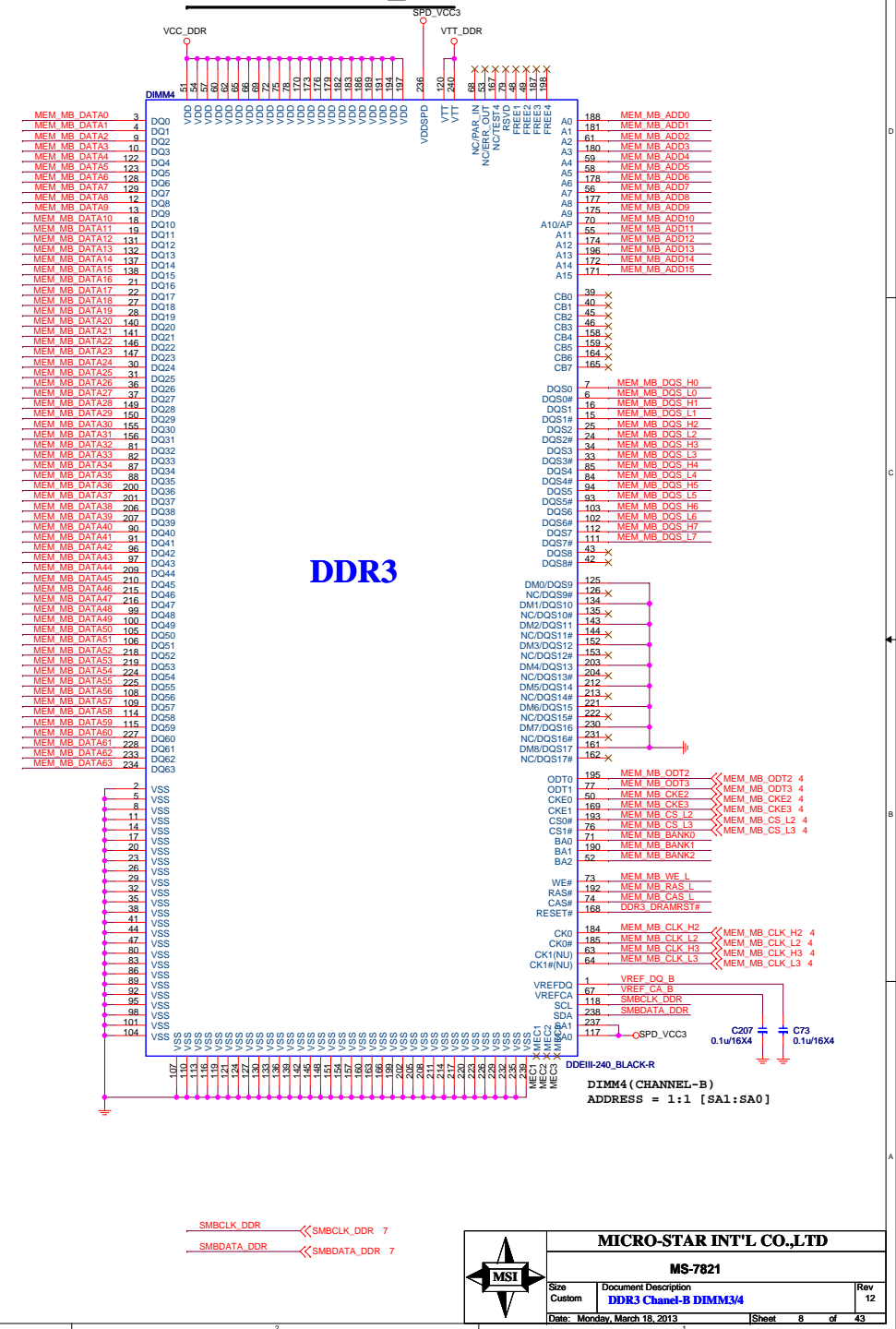


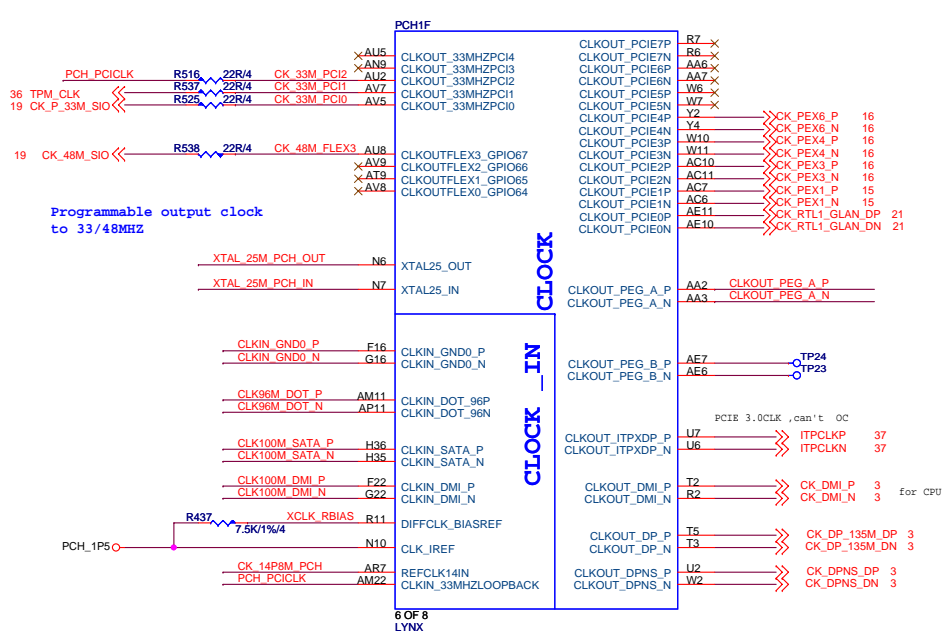
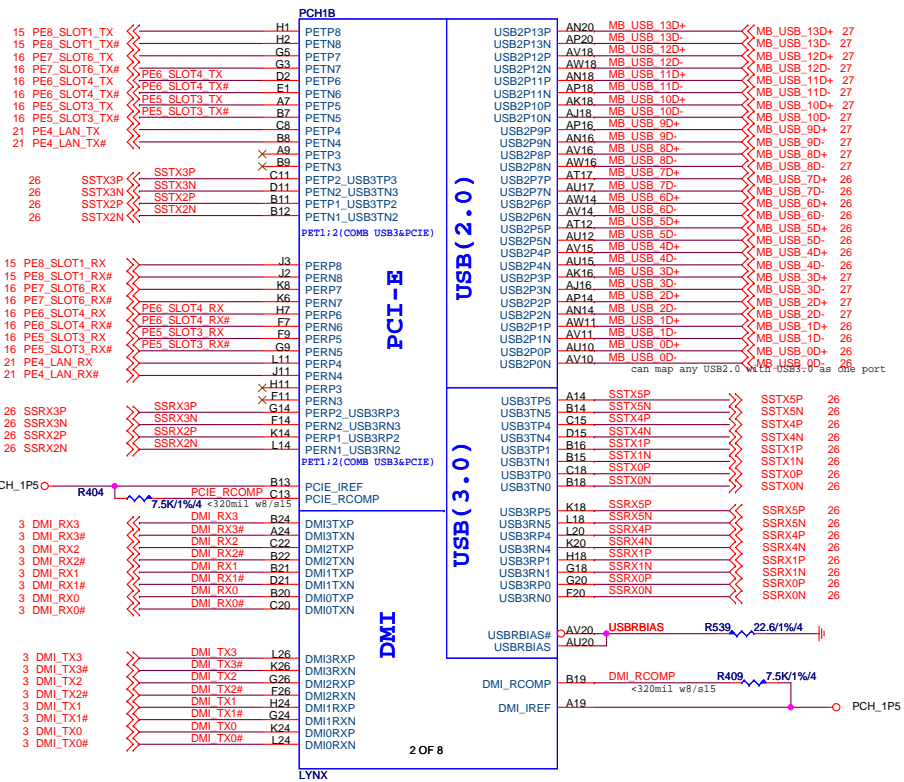


DDRIII DIMM_B0



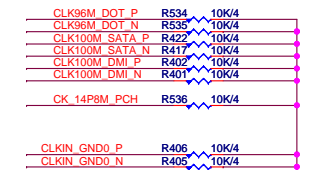
DDRIII DIMM_B1



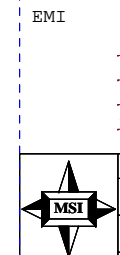
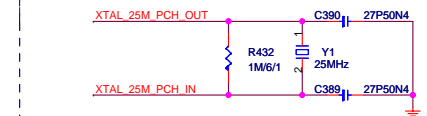
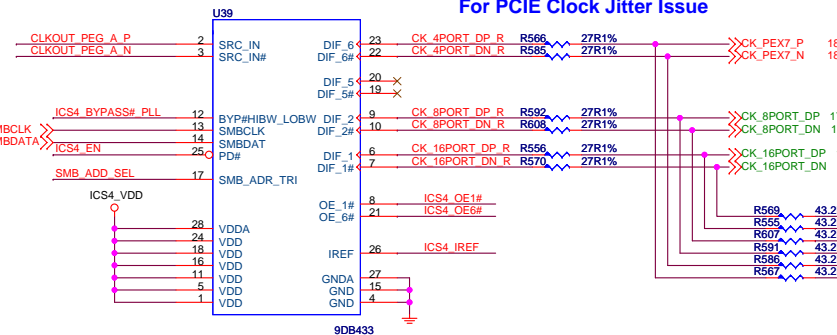


PCIE CLK BUFFER

no clock gen pull down



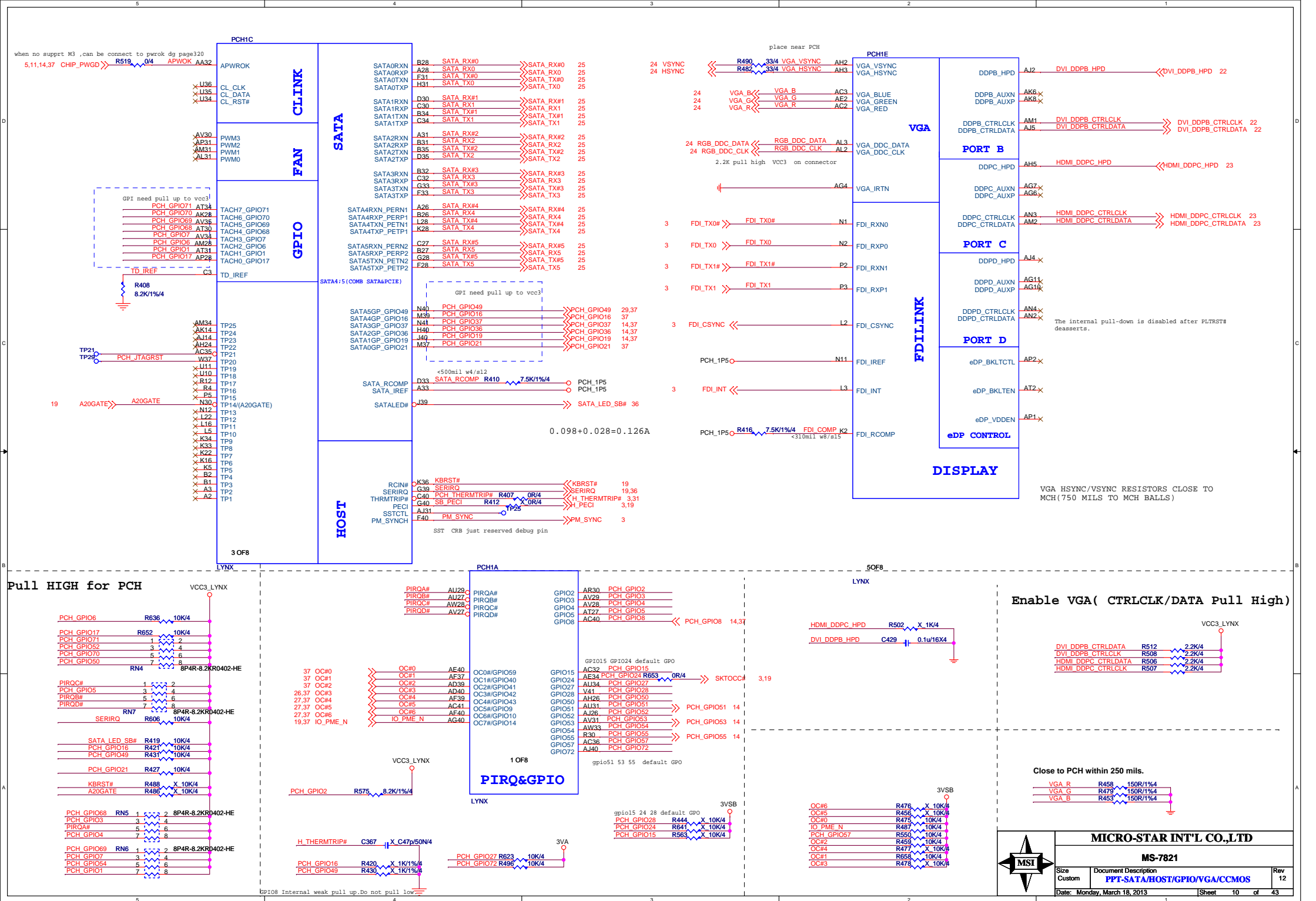
For PCIE Clock Jitter Issue

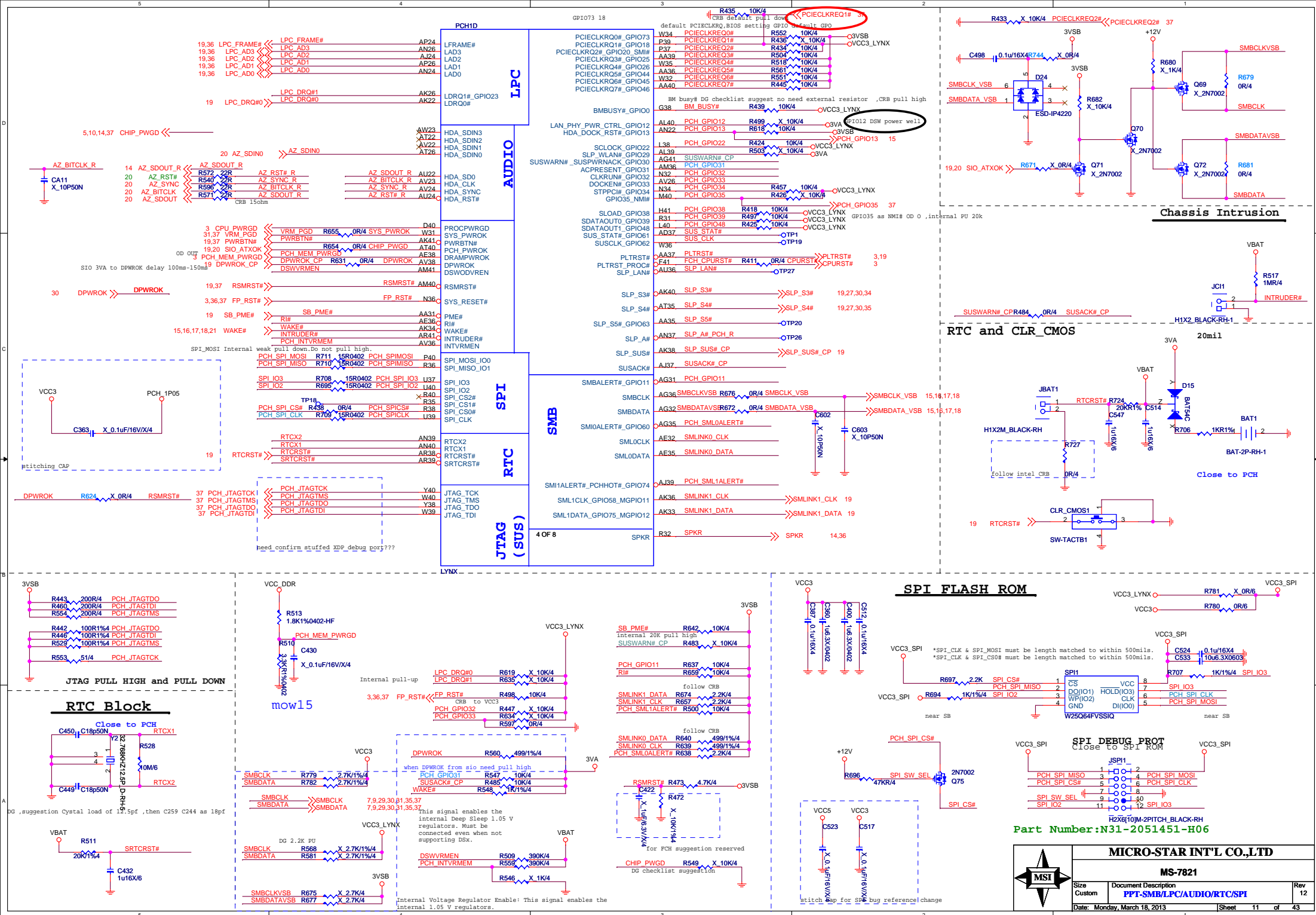


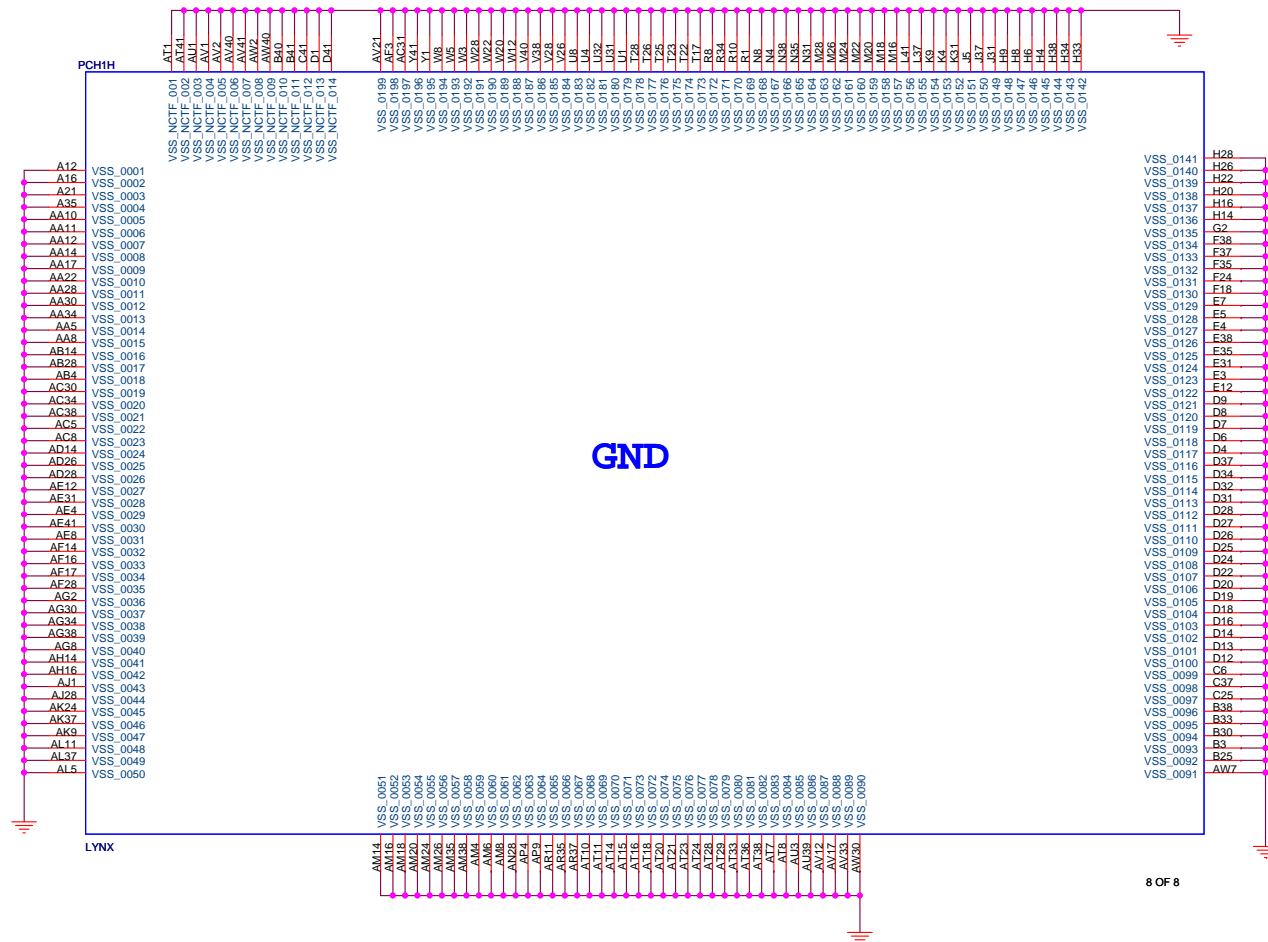
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Custom	PPT-PCI-E/DMI/CLK/USB20	12
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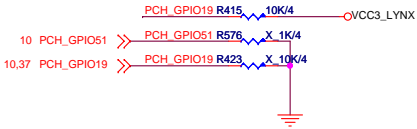




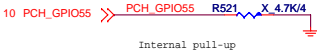
PCH Straps



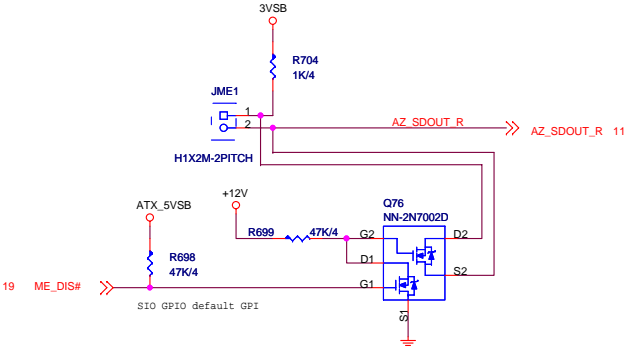
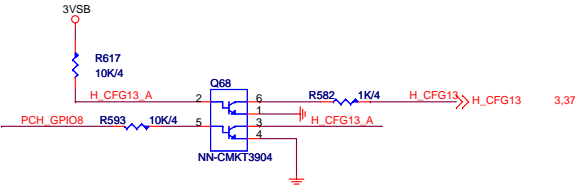
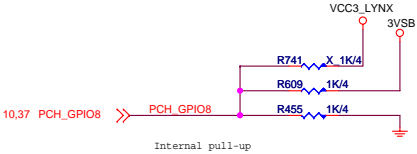
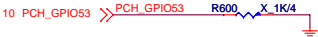
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1



Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



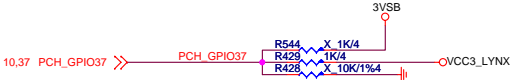
Connect to ground with 1k Ohm pull-down resistor.



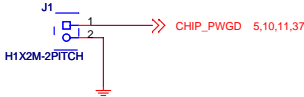
Default
Do not pull high.
Disable ME in Manufacturing Mode
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

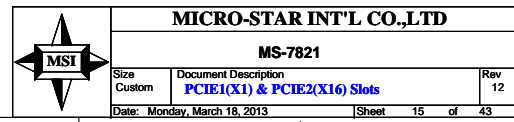


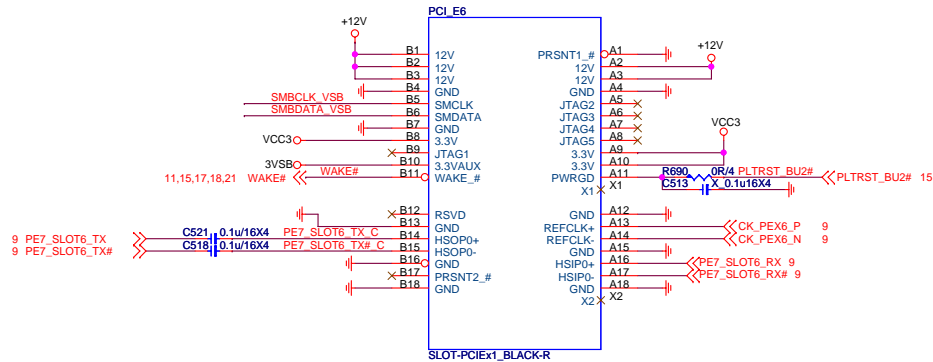
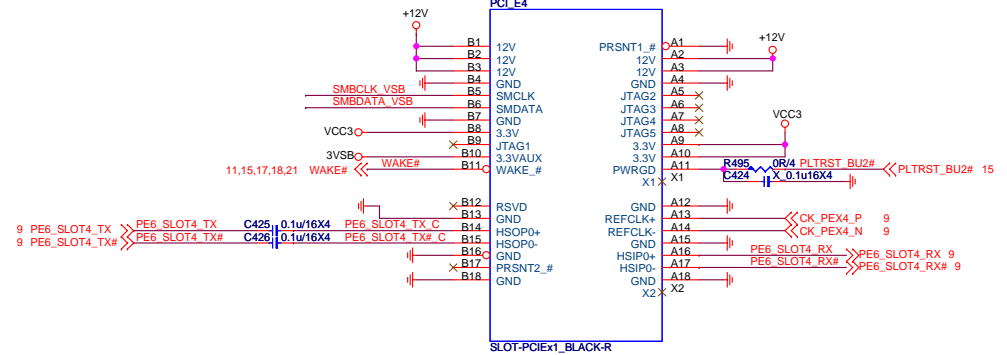
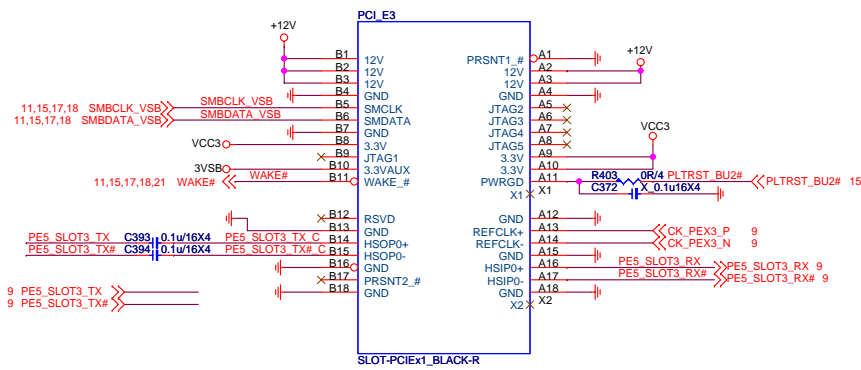
Internal weak pull down. Do not pull high.



GPIO37 Enable TLS:
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.







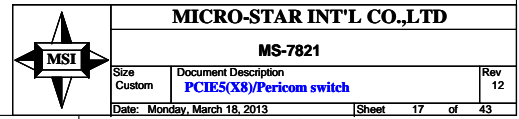
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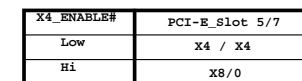
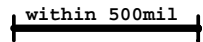
Size	Document Description	Rev
Custom	PCIEX(X1) & PCIE4(X1) Slots	12
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(Share with PCI_E x16 Slots)

(Share with PCI_E x16 Slots)



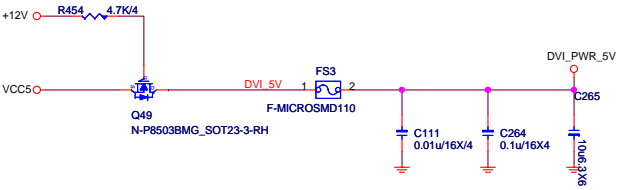
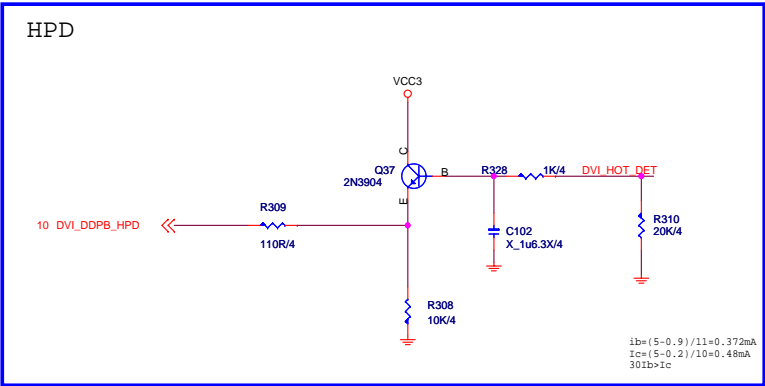
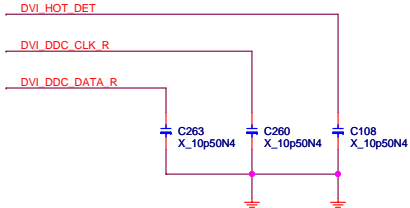
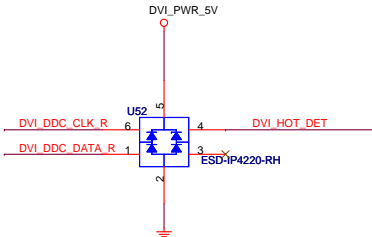
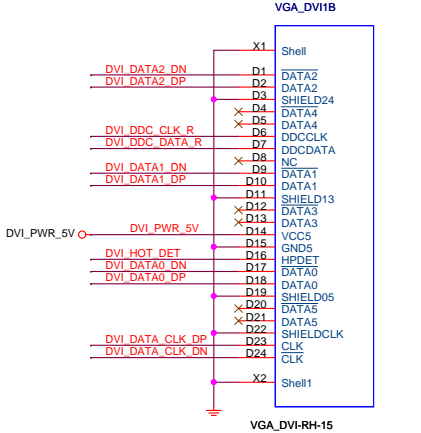
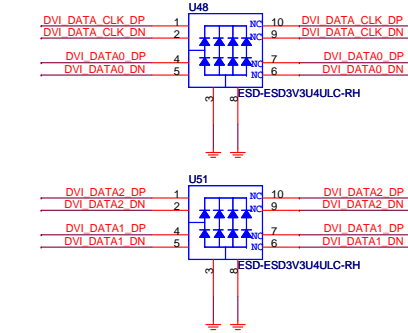
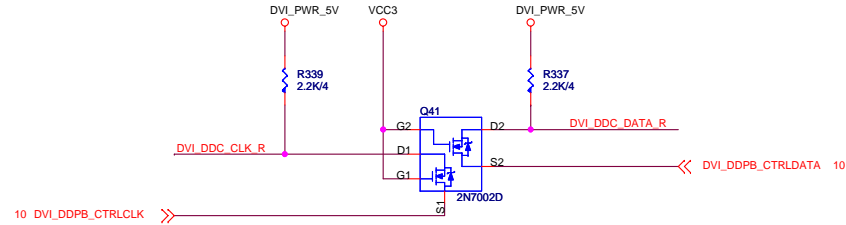
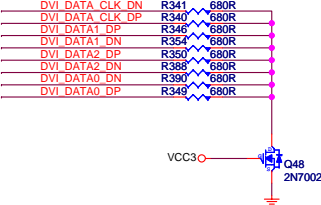
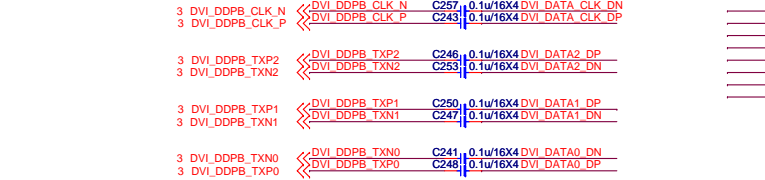
11,15,16,17 SMBCLK_VSB >>> SMBCLK_VSB
11,15,16,17 SMBDATA_VSB >>> SMBDATA_VSB



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Size Custom	Document Description PCIE(X4) & PCIE(X1) slots	Rev 12
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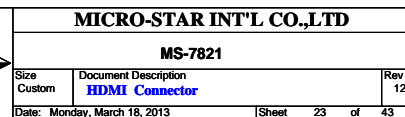
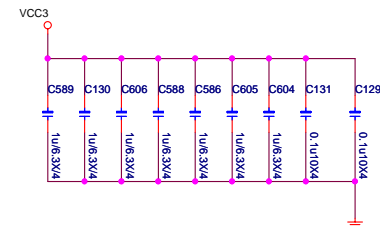
DVI level shifter



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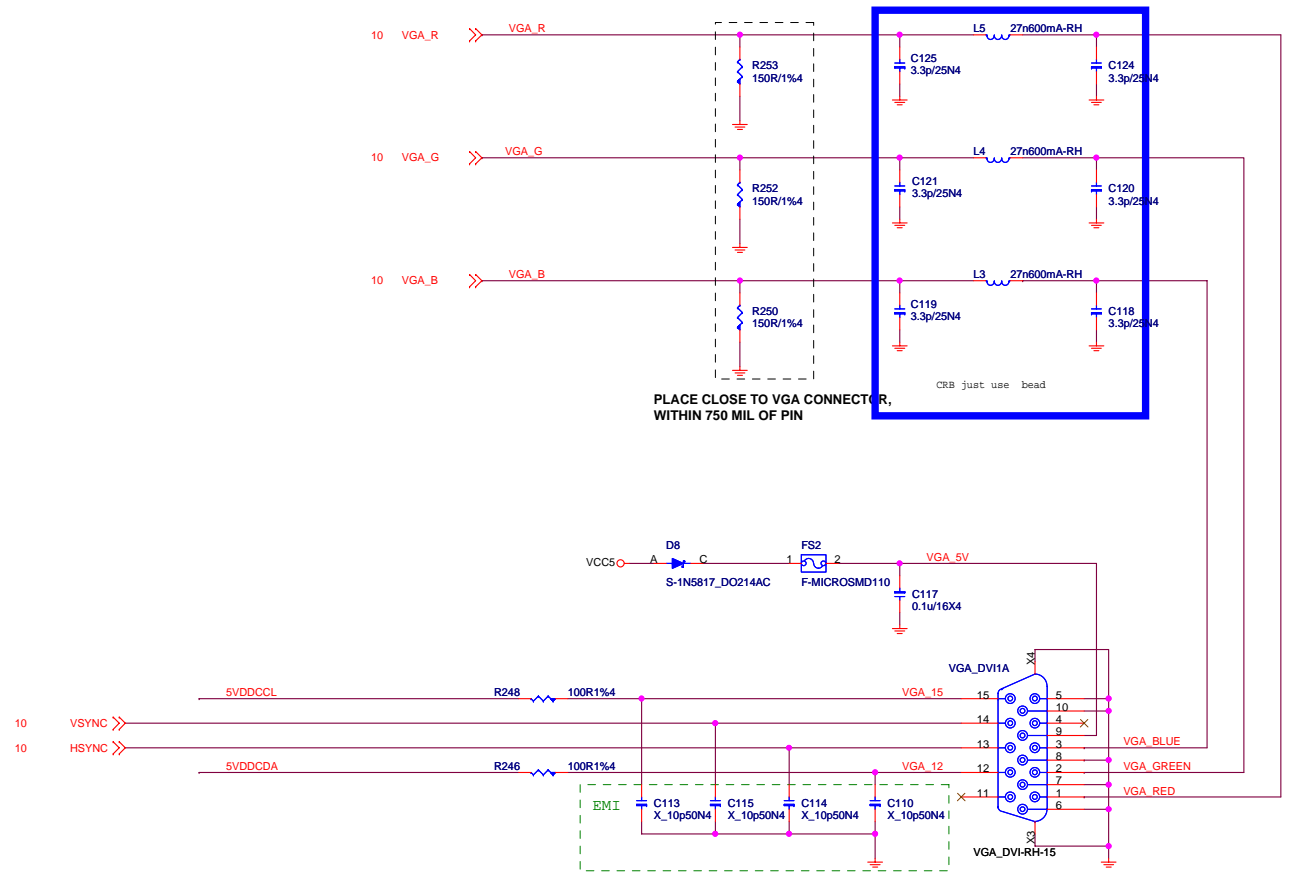
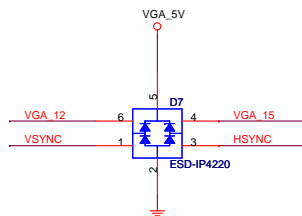
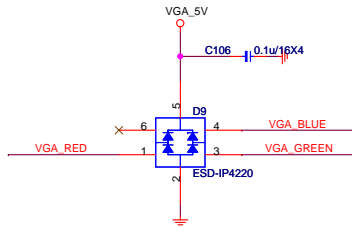
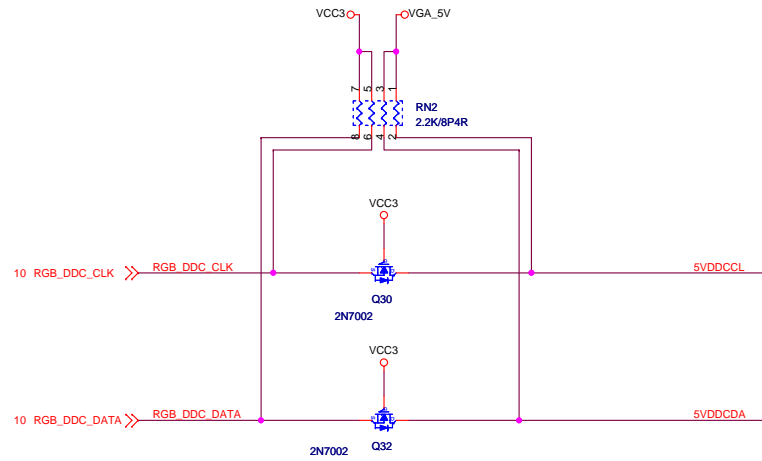
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D-Sub

Level shift

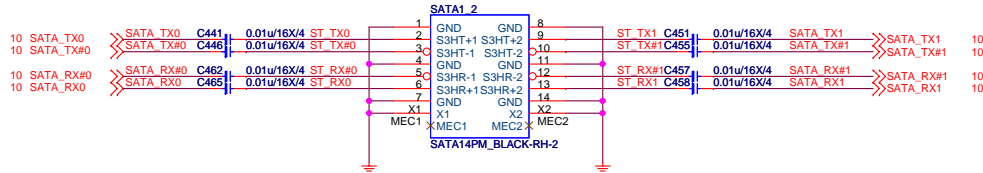


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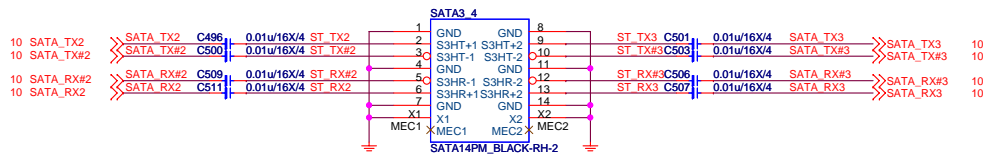
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Size Custom	Document Description VGA Connector	Rev 12
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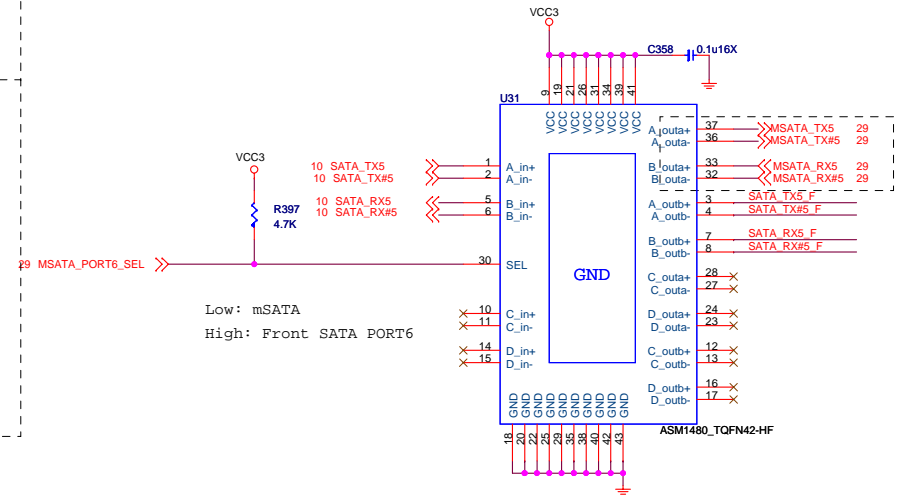
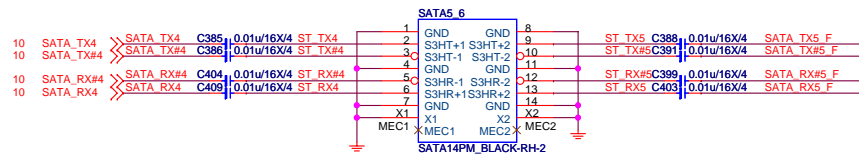
SATA1-2

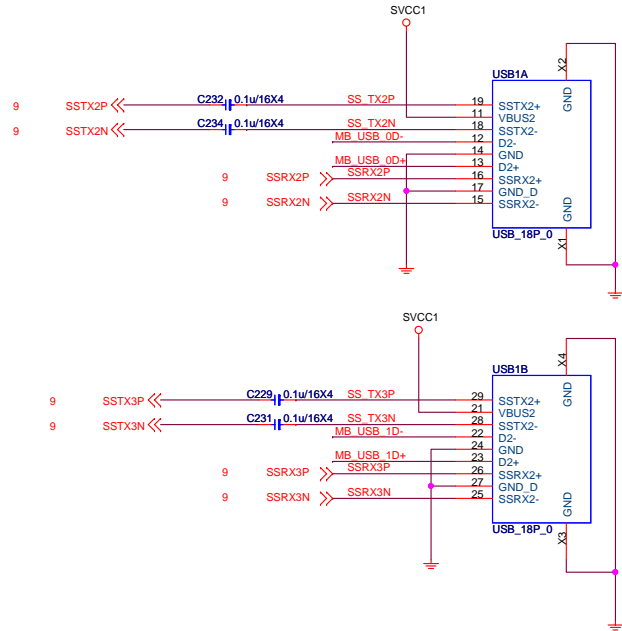


SATA3-4

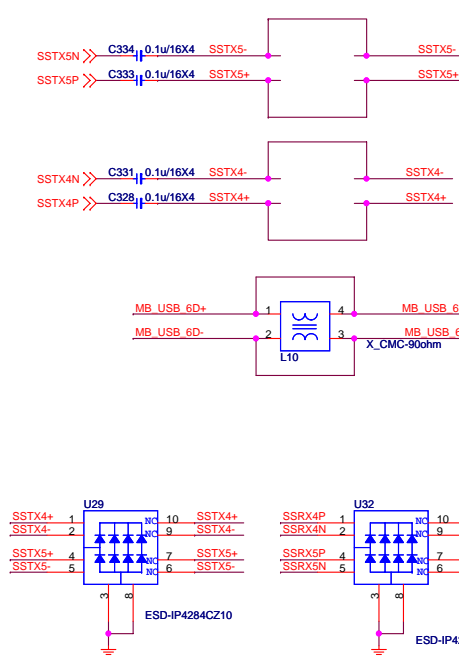


SATA5-6

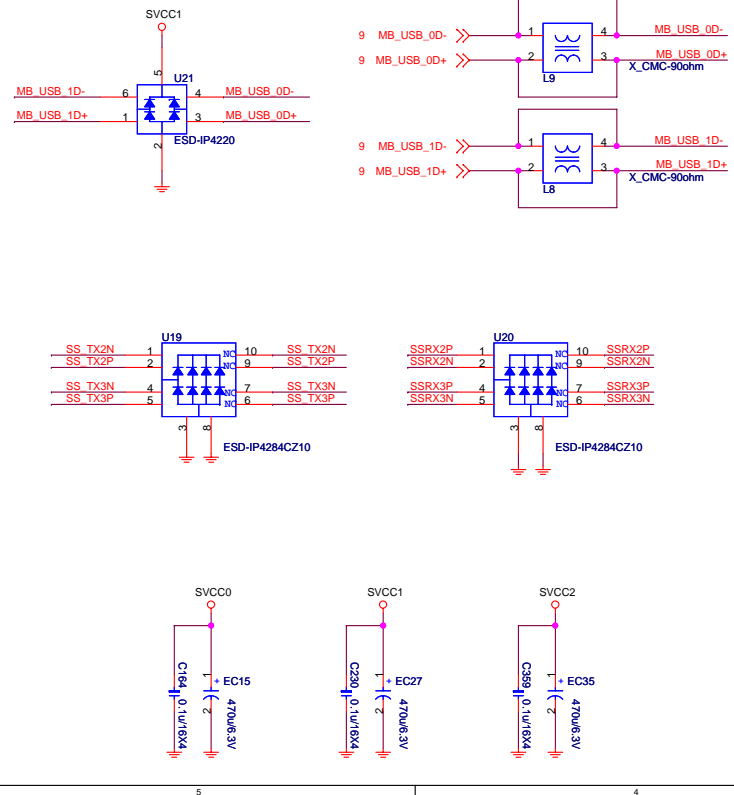




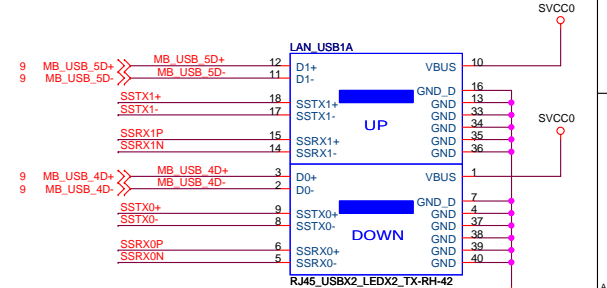
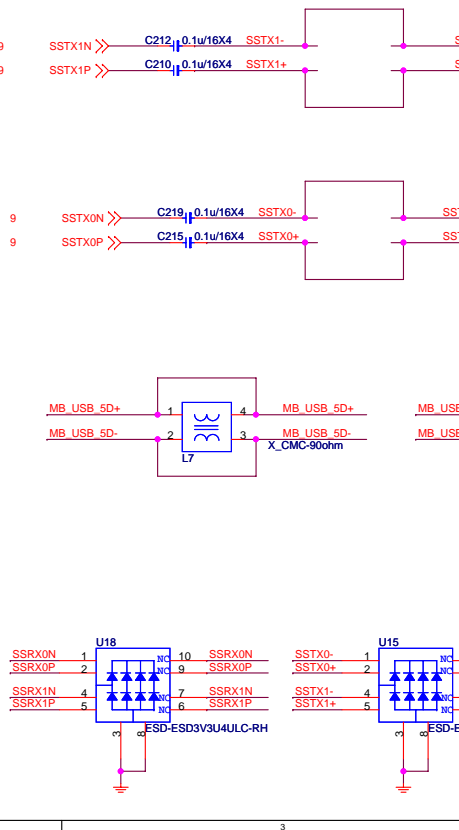
REAR USB30 PORT 2,3



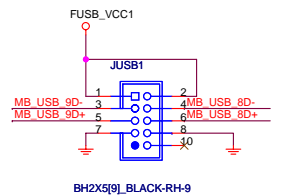
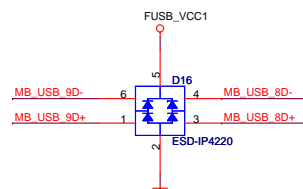
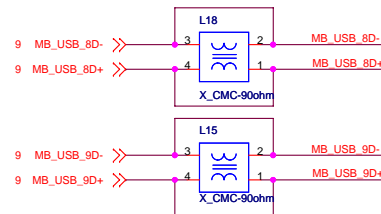
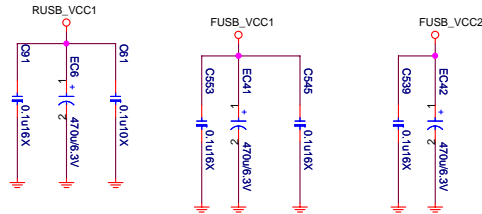
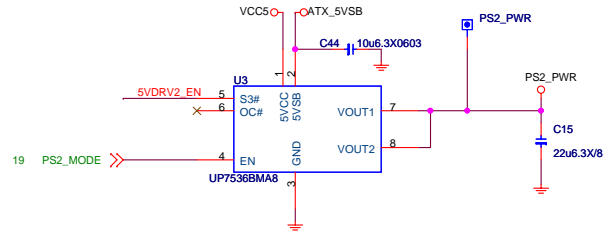
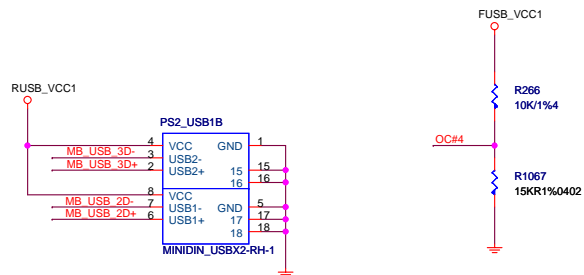
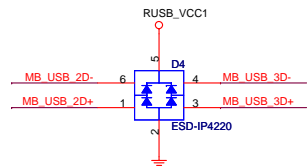
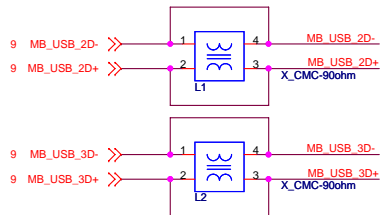
FRONT USB30 PORT 0,1



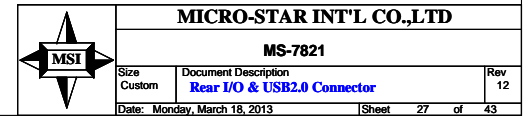
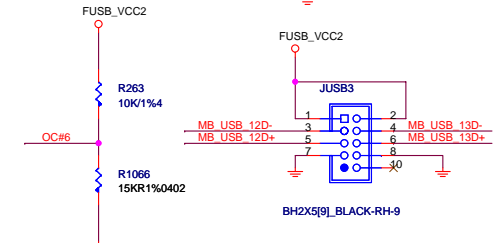
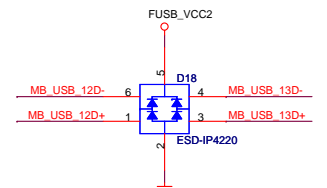
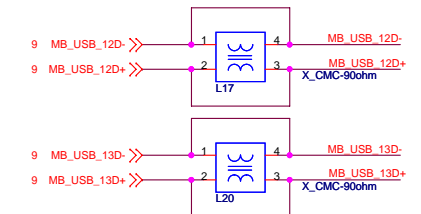
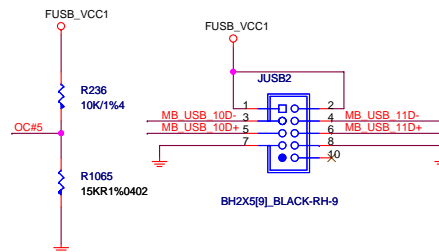
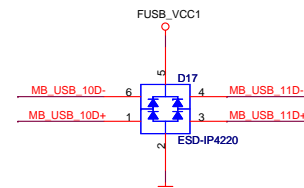
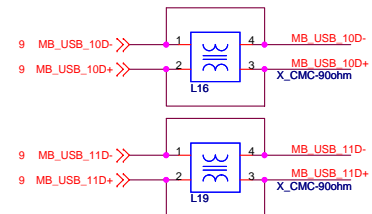
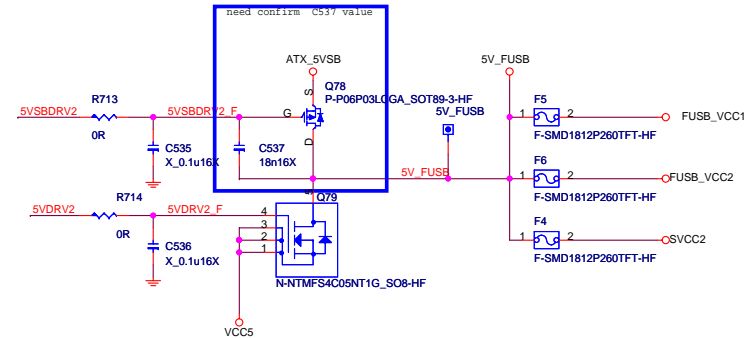
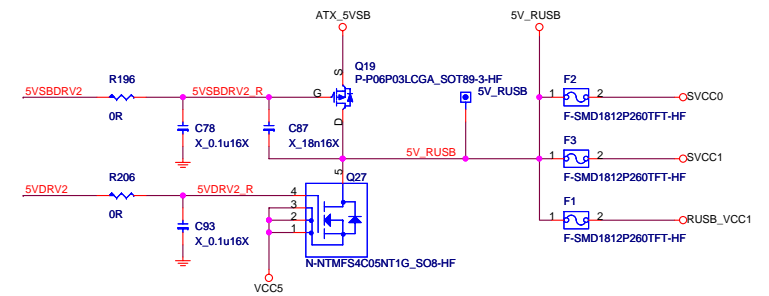
REAR USB30 PORT 4,5



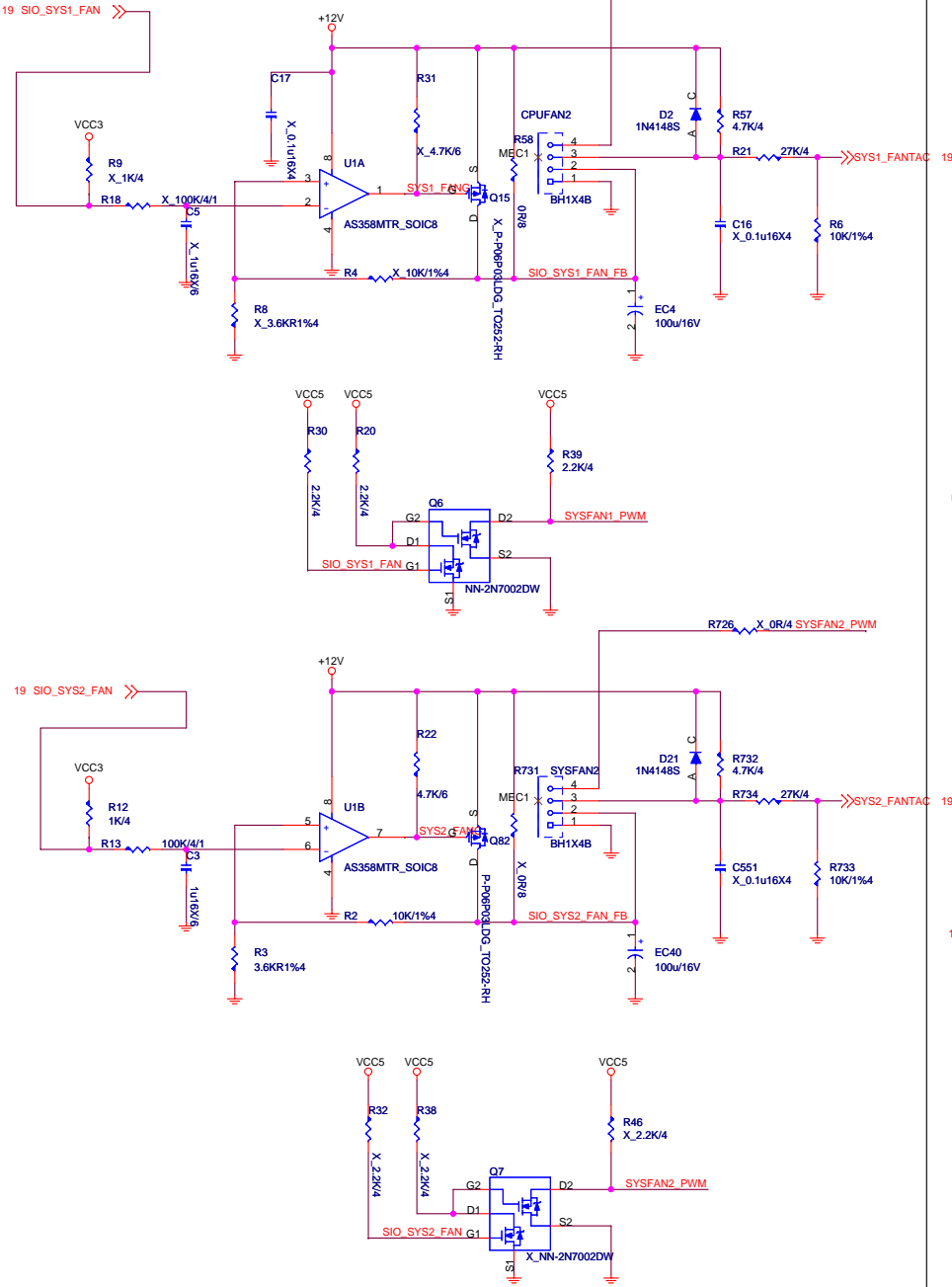
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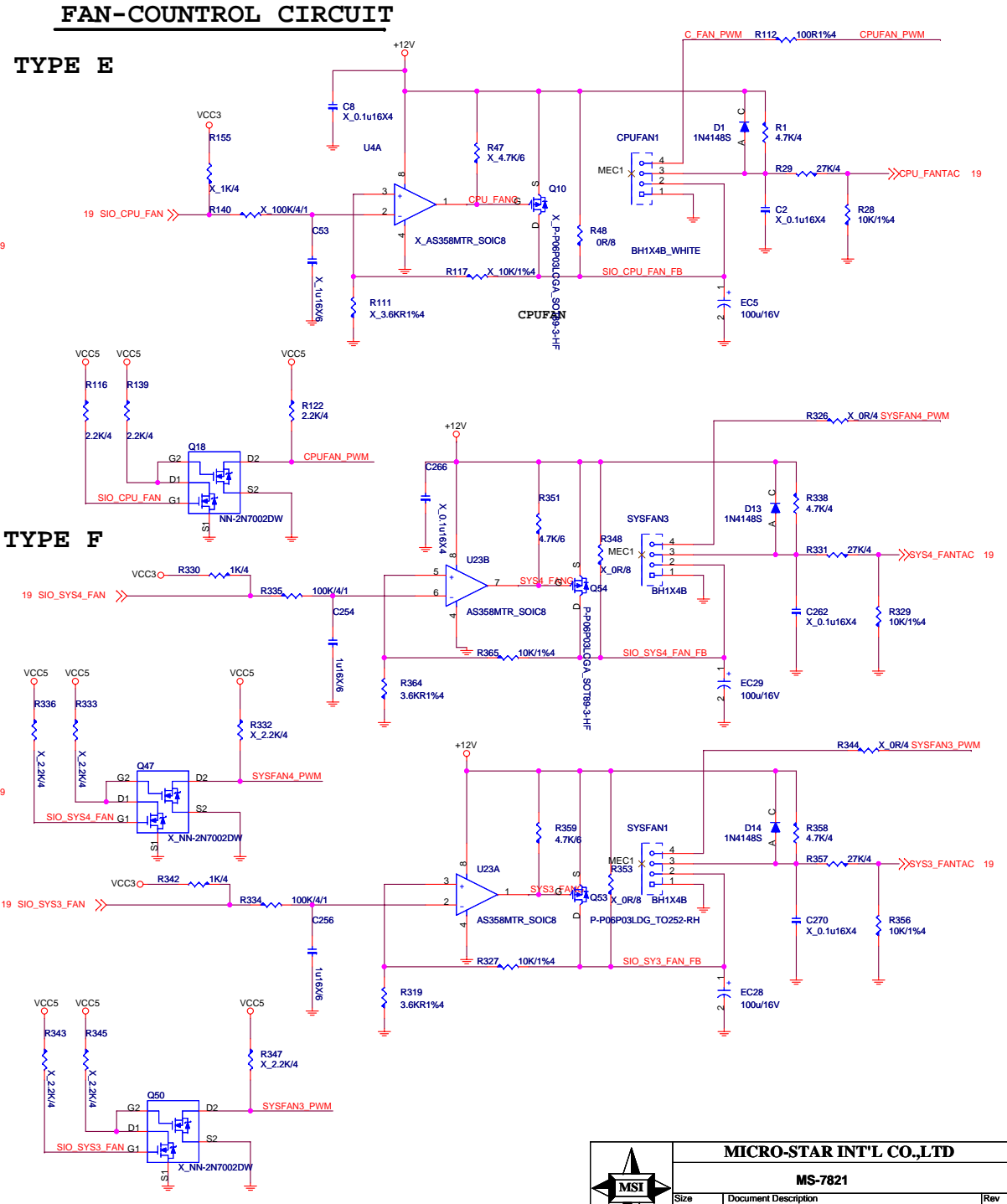
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OC#5	→	OC#5	10,37
OC#6	→	OC#6	10,37



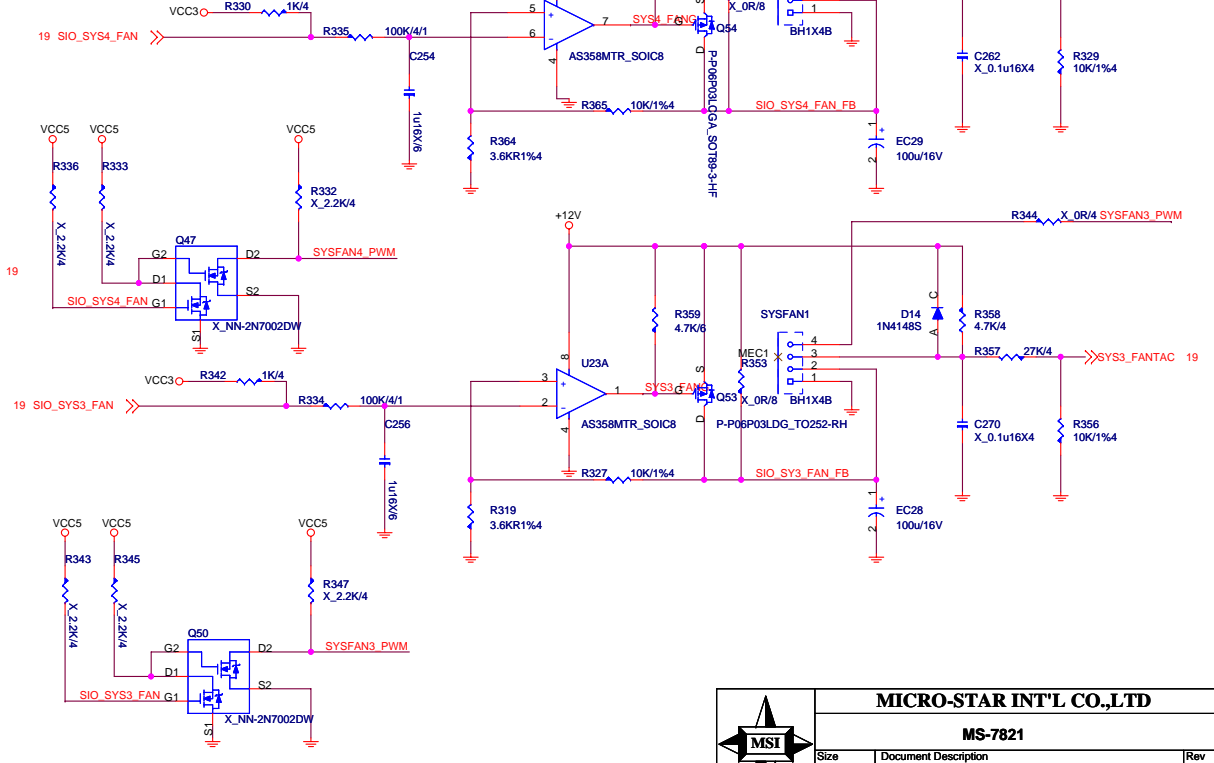
TYPE E



TYPE E



TYPE F

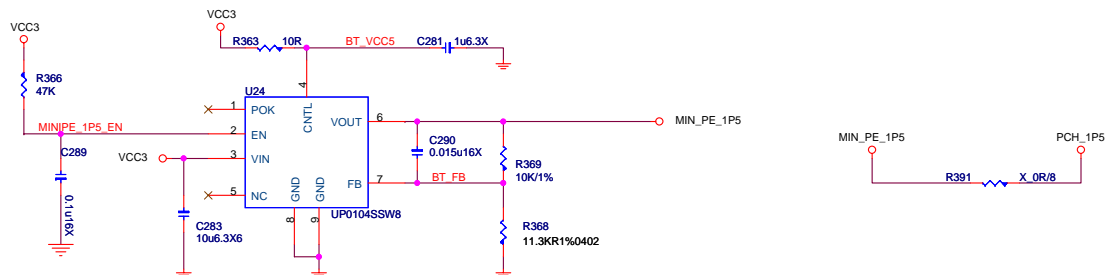
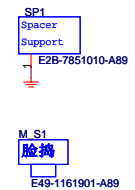


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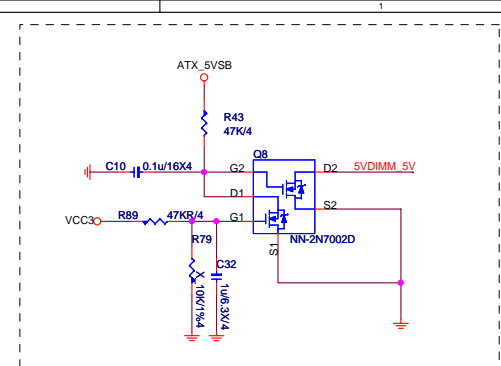
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VCC3, 1.5A
PCH_1P5, 0.5A



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Size Custom	Document Description MSATA	Rev 12
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[illegible][illegible]

patch power supply Vcc3 Vcc5 sequence

3V3 3V3

R687 X_0R/6

3V3

20mA

ATX_5VSB

C508 1u/6.3X/4

R684 47K/4

U43 UP0111A

VIN VOUT

EN GND FB

C510 X_0.1u/16X/4

R686 10K/1%4

3V3_REF

R685 3.09K/4/1

C504 C4.7u6.3X0603

3V3 3V3

3.389V

3V3

R678 X_47K/4

DPWROK EN

C505 X_0.1u/10

U42

1A 1Y

GND 2Y

2A 2Y

X_LVC2G14IDCKRQ1_SC70-6-RH

R679 X_3.09K/4/1

DPWROK

C495 X_0.1u/10

R669 10K/4

head reserved for PCH

ATX_5VSB

R703 X_10K/0402

R702

ATX_5VSB

C515 X_0.1u/10

0.82V

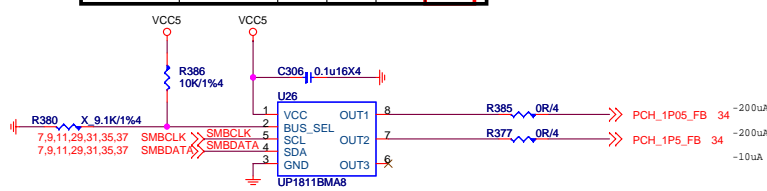
C520 X_0.1u/10

Q77

DPWROK_EN

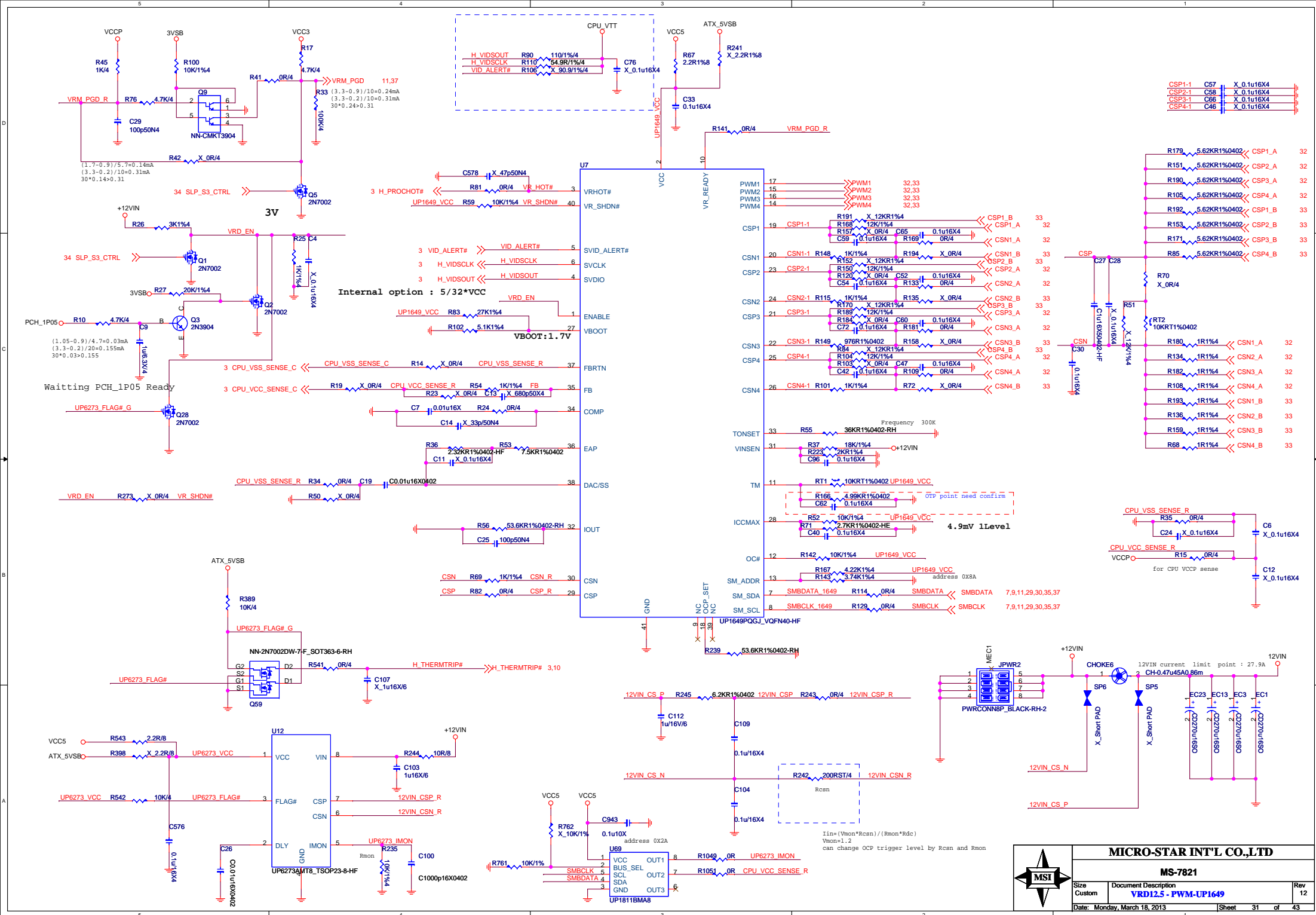
FOR DPWROK and 3V3 sequence (S5-->G3->S5)

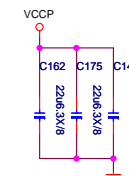
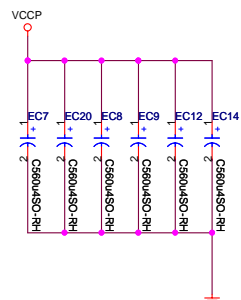
UPI VOLTAGE CONSOLE						
0x20: RH=10K, RL=OPEN						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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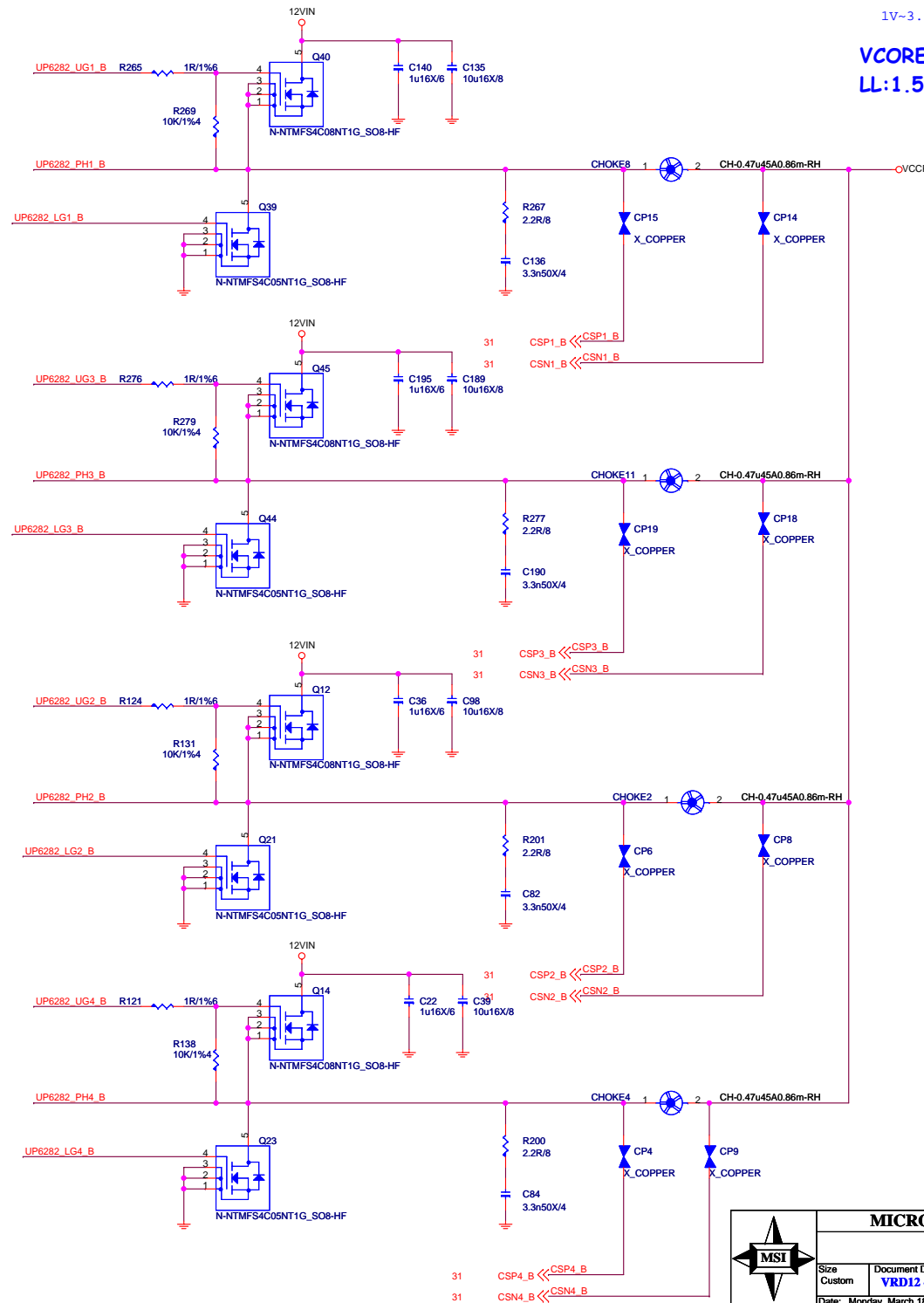
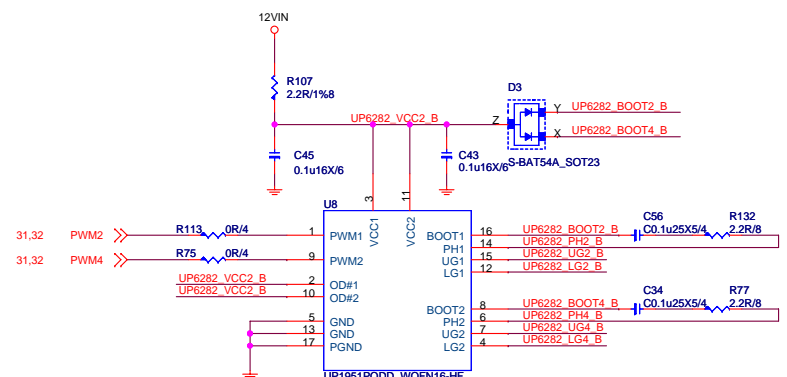
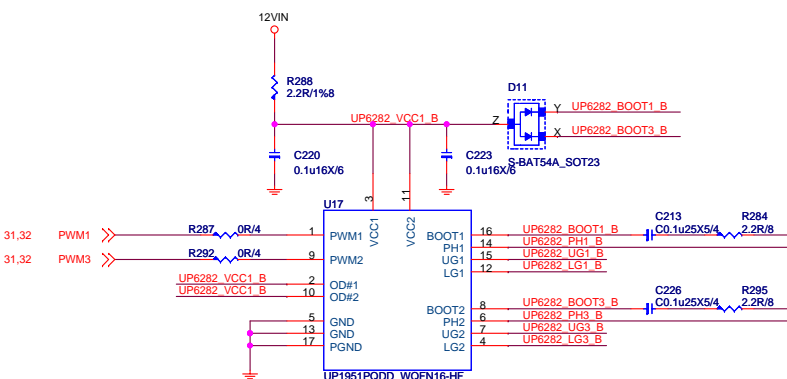



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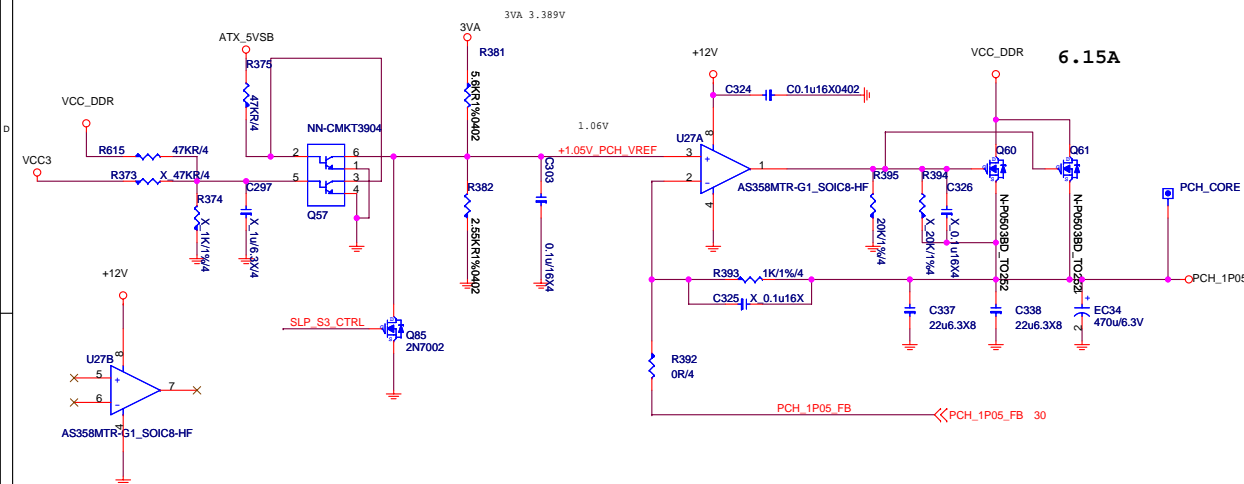
1V~3.04V/80A

VCORE 95A TDC:70A
LL:1.5m ohm

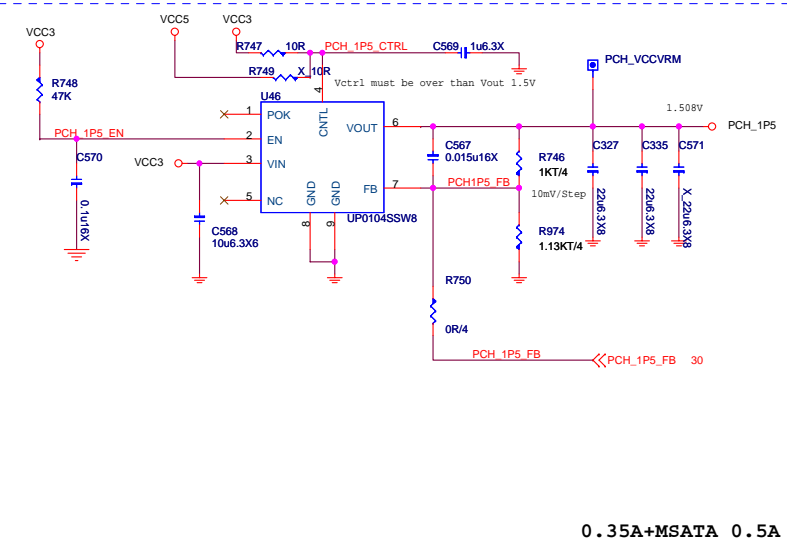


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1.05V_PCH

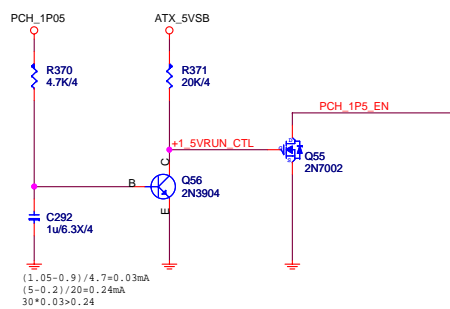


1.5VRUN

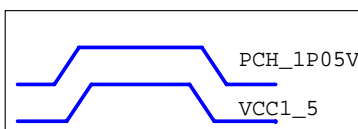


```
for 1.5V sequence control
```

Waitting PCH_1P05 Ready

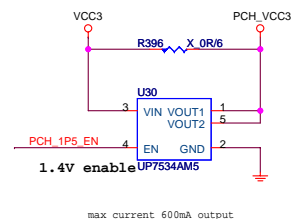


```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```

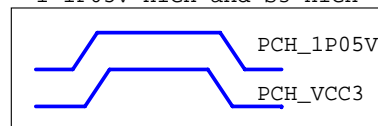


PCH Power:3.3V

0.188A



```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```

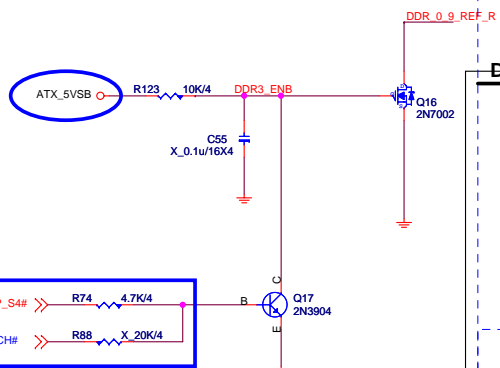


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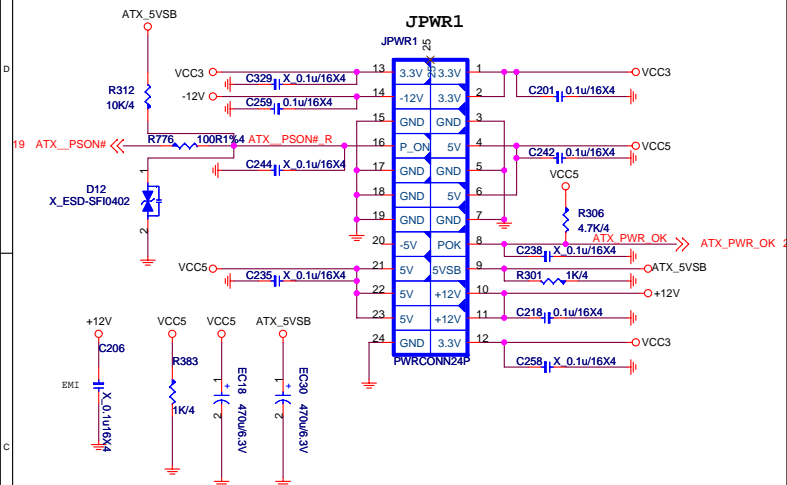
Size Custom	Document Description VTT POWER- uP1513	Rev 12
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$OCP ((5*10v6*R758/(3.4/2)m\ ohm=36.47A>22.3*1.5A$

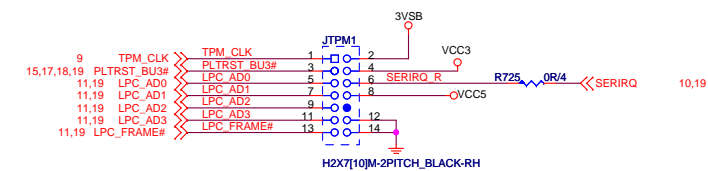
[illegible]

Size Custom	Document Description DDR Power -1-Phase	Rev 12
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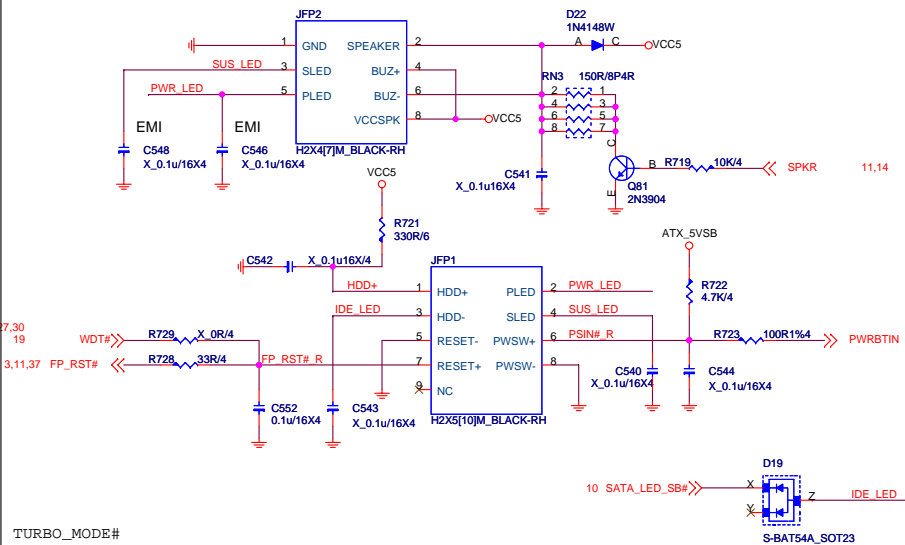
ATX POWER CONNECTOR



TPM

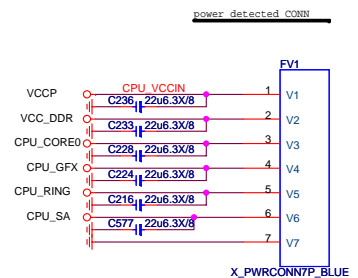
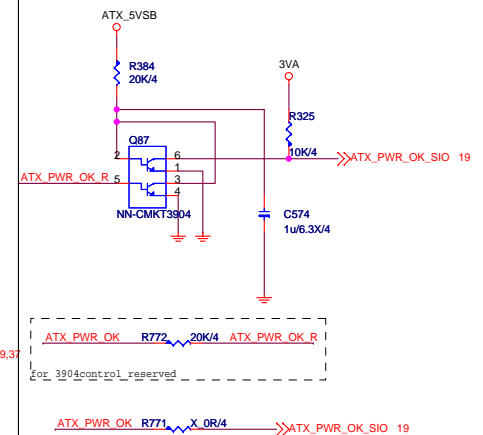
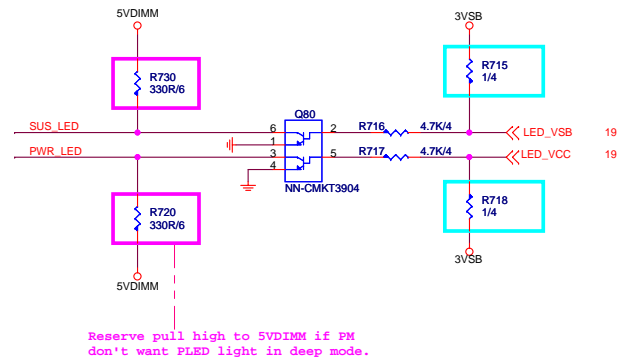


FRONT PANNEL



TURBO_MODE#
Default: Low,disable OC
Push Bottom: high,Enable OC / Turn on LED

LED (for NCT6799D)

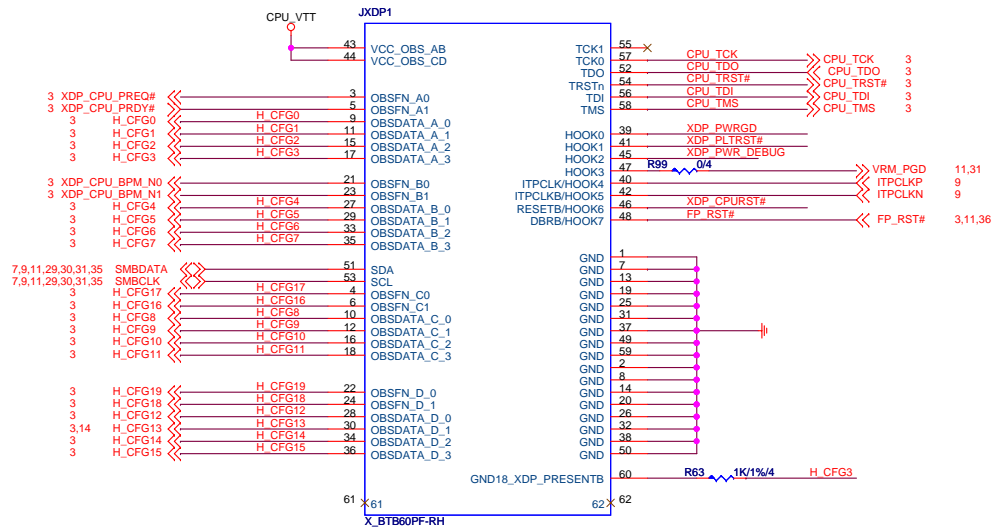


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Reserve debug port 5020



CPU_TDO R66 51/4 PCH_1P05
PLACE NEAR XDP CONNECTOR

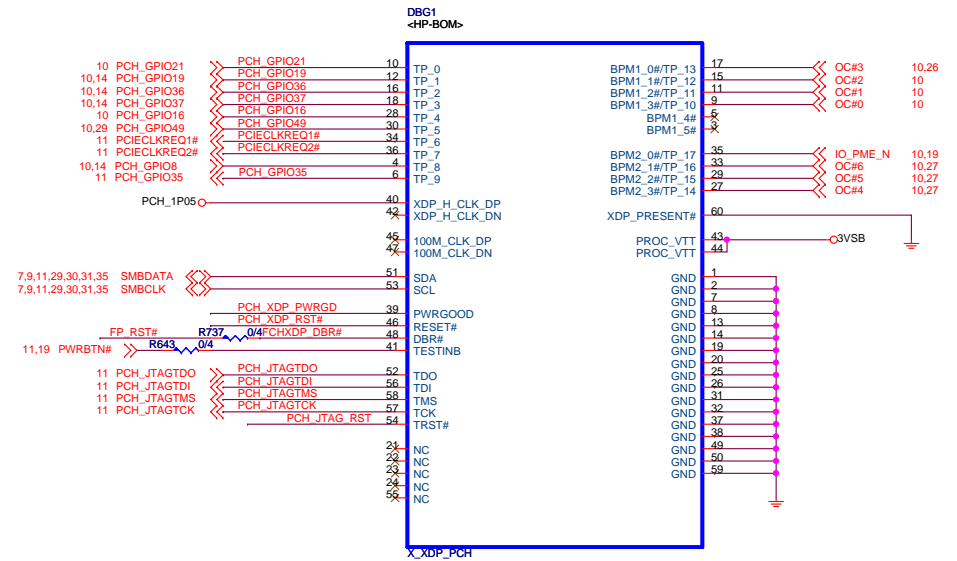
19,36 PWRBTIN >> PWRBTIN R186 0/4 XDP_PLTRST#
3 PWR_DEBUG >> R211 0/4 XDP_PWR_DEBUG

mo15

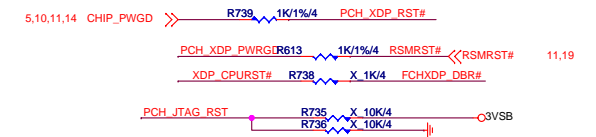


3 CPURST#_R >> R96 1K/1%/4 XDP_CPURST#

PCH XDP



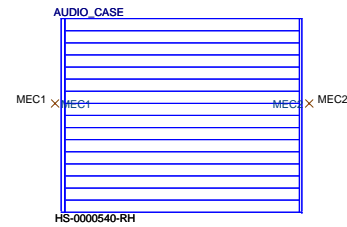
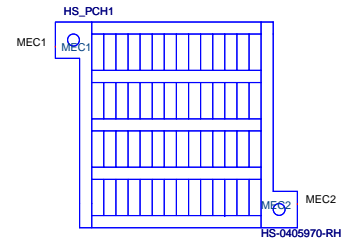
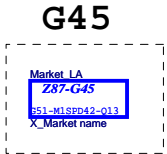
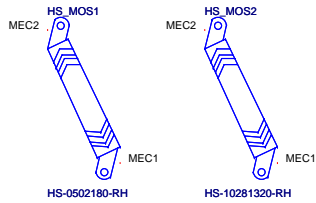
PCH XDP PWRGD/RESET



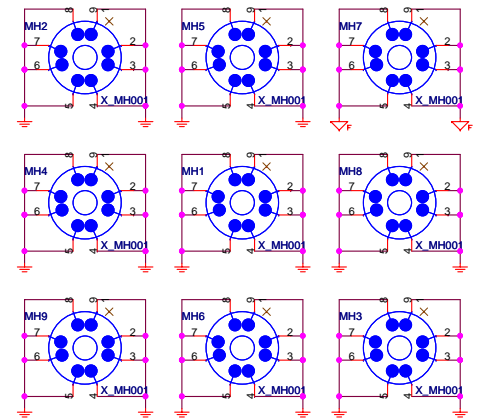
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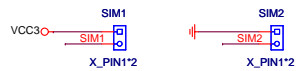
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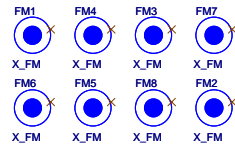
Mounting Holes



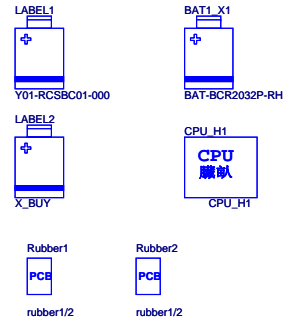
Simulation



Optical Fiducial Marks-120



PCH XDP PWRGD/RESET



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



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